High Frequency Noise Characteristics of RF MOSFETs in Subthreshold Region

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Abstract - **High frequency noise characteristics of 0.13um and 0.18um n-type MOSFET across a full range of bias conditions is presented in this paper. Focus is mainly on nMOSFET's behavior in "off" state, which is not predicted accurately by existing commercial models. This is a region especially important for full-chip RFCMOS design. In this paper, noise parameters (NFmin, RN, Γopt) up to 6GHz are investigated in detail. From the device perspective, the power spectral density of channel noise and induced gate noise is also studied to understand how MOSFETs actually operate from strong inversion to weak inversion and depletion.**

INTRODUCTION

Due to the continued scaling of CMOS and the resulting increase of Ft and Fmax, CMOS has found more and more applications in RF circuits. Research has been focused on the adoption of CMOS into the RF wireless world, because it has the advantage of being low cost, with a high level of integration possible. To design a full chip RF transceiver, it is important to have accurate models for the analog behaviors of MOSFETs, such as flicker noise, thermal noise and nonlinearity as the design turnaround time is important.

While the high frequency noise model for bipolar devices is quite mature, the accurate prediction of MOSFET noise behavior has been lacking, partly due to the lack of interest. In the past, noise models for MOSFETs can be found in SPICE and BSIM3 models. These models, however, can not predict the noise behavior accurately, because of the absence of induced gate noise modeling. Recently, BSIM4[1] and Philips MOS11[2] models have included the induced gate noise model. However, these models only focus on weak to strong inversion. The research of noise behavior in the subthreshold region of the MOSFETs has been ignored. Indeed, the "off" state applications can be found in RF circuits, such as LNAs with variable gain and mixers. In this paper, we will show the noise parameters of n-type MOSFETs with the gate bias down to -0.4V with focus on 5GHz. Measurement was done on two generations of technologies to show the consistency. We also extract the noise power density of channel noise and induced gate noise to understand how they change with the gate bias.

OVERVIEW OF EXISTING MODELS

BSIM4 and Philips MOS11 are the two publicly available models with the induced gate noise model included. To compare both with the traditionally accepted Van der Ziel model, it is implemented in our internal circuit simulator. Fig. 1a shows the topologies of Van der Ziel[3] and MOS11 models. They basically share the same topology. The MOS11 model however, uses different equations for the channel noise(Sth) and the induced gate noise(Sig). Both models set a correlation factor for the two noise sources as they originate from the same source. Fig. 1b shows the topology of the BSIM4 model. Unlike the previous two, it is modeled as two uncorrelated noise sources. The channel noise is split into two parts: one as a current noise source and the other as a voltage noise source. The induced gate noise is generated from the voltage noise source put at the source side through the gate coupling. In the model, this voltage source is embedded into the source resistance. Fig. 2 and Fig. 3 show the simulated minimum noise figure of each model. For BSIM4 and Van der Ziel, we have tuned the model parameters to fit the measurement data down to 0.5V. For Philips MOS11, the simulation was

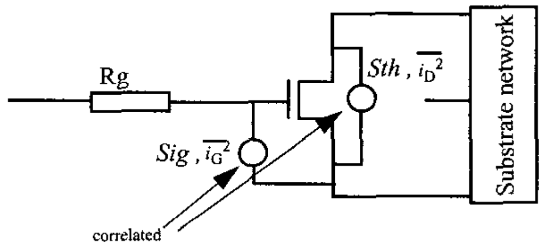

Fig. 1a Topologies of the Van der Ziel model and Philips MOS11 model. Both model share the same topology, but with different equations for channel noise and induced gate noise. Both noise sources are correlated.

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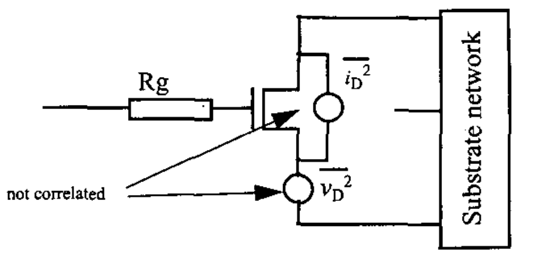

Fig. 1b Topology of BSIM4 model with tnoimod=1. The drain noise is split into two uncorrelated noise sources. The induced gate noise is generated from voltage noise source put at the source side through the gate coupling.

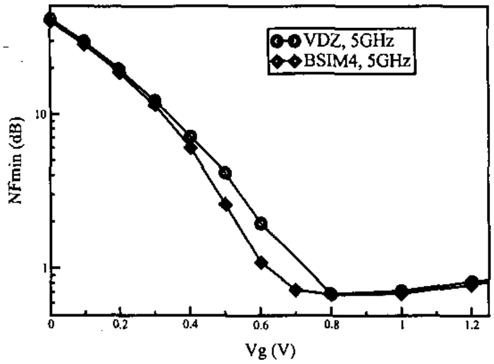

Fig. 2 Simulated NFmin versus gate bias Vg using Van der Ziel and BSIM4.2.0 model. Data was extracted at 5GHz. Model parameters were finely tuned to match the measurement data.

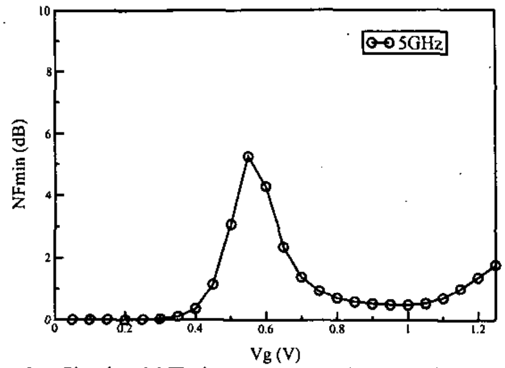

Fig. 3 Simulated NFmin versus gate bias Vg using Philips MOS11 model level 1101. Data was extracted at 5GHz. Simulation was done in Agilent ADS. No model parameter fitting is necessary.

done in Agilent ADS. Since Philips MOS11 is physics based, no fitting is necessary. In Fig. 2, NFmin is plotted against Vg at 5GHz. NFmin first changes slowly and then sharply increases with decreasing Vgs. Noise resistance Rn also shows the same trend. It should be noted that an increase of NF does not imply an increase of noise source power. However, in this case, the increase of NFmin is indeed coming from the higher induced gate noise power. In the Van der Ziel model, the induced gate noise power is inversely proportional to the transconductance. On the other hand, the channel noise power is proportional to the transconductance, and thus the induced gate noise will dominate at low gate bias, since the gain of the MOSFET in subthreshold region stays very much unchanged. The combination of these two phenomena causes the sharp increase of NFmin with decreasing Vgs. Similarly, the induced gate noise in BSIM4.2.0 has caused the very high NFmin at low gate bias. Fig. 3 shows the simulated NFmin using the Philips MOS11 model level 1101. As can be seen, it shows similar behavior in weak to strong inversion. In the subthreshold region, however, it predicts almost 0 dB for NFmin. Similar to the previous two models, the channel noise is extremely low at low gate bias and thus the trend is determined by the induced gate noise. In the MOS11 model, the induced gate noise is expressed as

$$S_{ig} = \frac{\frac{1}{3}N_T T\left((2\pi f C_{ox})^2/g_m\right)}{1+0.075((2\pi f C_{ox})/g_m)^2}$$

At sufficiently high frequency, Sig is proportional to gm when gm is very small. That is why a very low NFmin is predicted at low gate bias.

NOISE MEASUREMENT RESULT

All measurements were performed using an ATN noise parameter measurement system. Noise parameters were extracted from 16 sets of noise figure data with different input impedance states. Various sizes of MOSFETs with gate length of 0.18um were measured. The data of a very large device with a width of about 1000um is presented here. While the devices with smaller sizes show the same trend, large devices allow more accurate measurement, especially at low gate bias. The variation of extracted NFmin across frequency for the large device is about +/- 0.1dB at high gate bias and +/- 0.2dB at low gate bias. The better accuracy of a large device is possibly due to the Γopt that is closer to the available impedance states of the input tuner. To verify our results, the noise figure parameters of a 0.13um MOSFET at different width is also shown.

Fig. 4 shows NFmin versus gate bias for a device with threshold voltage of about 0.6V. In strong inversion, NFmin is not sensitive to either drain bias or gate bias. As Vg approaches Vt, NFmin sharply increases. This is consistent with published results. As the device is driven into subthreshold region, however, NFmin becomes saturated. Fig. 5 shows noise resistance Rn versus gate bias. It has the same trend as NFmin, namely, it saturates to a constant in the subthreshold region. If we look closely, it can be seen that Rn actually drops slightly before it saturates. The same trend can be seen in Fig. 4. Also, we can see that Rn increases slightly with the drain bias since Rn is solely determined by the channel noise. The spreading of the NFmin curves with drain bias in the subthreshold region is also observed in Fig. 4. However, the trend is not clear. NFmin is determined by channel noise, induced gate noise and the correlation factor. Also, the extracted NFmin is more sensitive than Rn to experimental error and thus this trend is yet not conclusive.

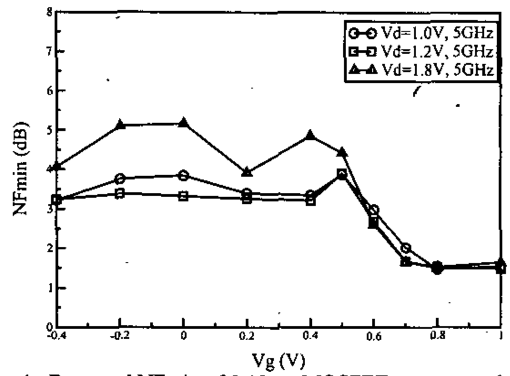

Fig. 4 Extracted NFmin of 0.18um MOSFET versus gate bias Vg. Drain bias varies as 1.0v, 1.2V and 1.8V. Data was extracted at 5GHz.

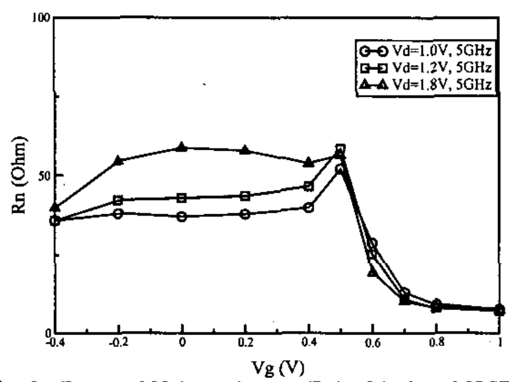

Fig. 5 Extracted Noise resistance (Rn) of 0.18um MOSFET versus gate bias Vg. Drain bias varies as 1.0V, 1.2V and 1.8V. Data was extracted and 5GHz.

From the design perspective, it is also important to know what the Γopt is because it determines the trade-off of power and noise matching. The data is shown in Fig. 6. Vd is set at Vd=1.2V and the frequency sweep is from 0.3GHz to 6GHz. Γopt moves from the first quadrant into the second quadrant as frequency increases. For small devices, Γopt will be in the first quadrant and close to the 0 Ω circle. As Vg decreases, Γopt moves away from the 50 Ω center. Similar to NFmin and Rn, it saturates as the device is in the subthreshold region.

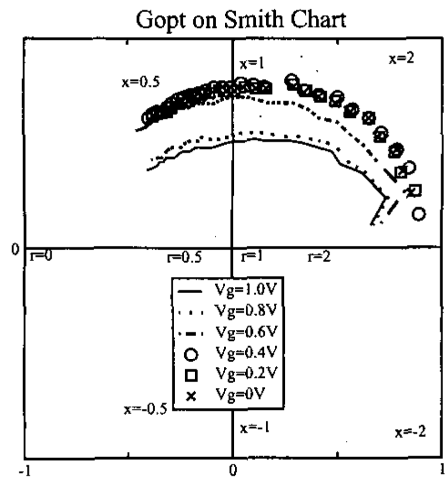

Fig. 6 Extracted Γopt of 0.18um MOSFET on Smith chart. Frequency swept from 0.3GHz to 6GHz. Drain bias is at 1.2V.

To confirm our result, a 0.13um MOSFET was also measured. The result is shown in Fig. 7. At Vd=1.0V, the extracted NFmin and Rn at 5GHz have shown the same trend as the 0.18um device. As can be seen, NFmin has similar magnitude as the 0.18um device. The decrease of NFmin with scaling is not as obvious. The larger noise resistance here is due to the smaller size of the device.

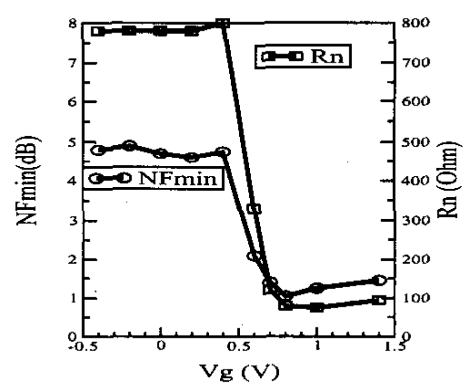

Fig. 7 Extracted NFmin and Rn of 0.13um MOSFET. Drain bias is at 1.0V. Data was extracted at 5GHz.

CHANNEL NOISE AND INDUCED GATE NOISE

Noise parameter representation is a convenient tool for design because the output noise behavior of a two port element can be easily described. However, it tells very little about the device itself. To understand the device more, it is more useful to look at the power density of the noise sources. With the channel and induced gate noise topology as in Van der Ziel model, the power density can be transformed from the noise parameters using simple two-port y-parameter representation. The results are shown in Fig. 8-10. In Fig. 8, the power spectral density of the channel noise at 2GHz and 5GHz is plotted against gate bias Vg. The power density drops with decreasing gate bias as predicted by most of the models. It then stays unchanged in the subthreshold region. While the channel noise is known to be frequency independent, we can notice that this is the case only in strong inversion. As the device is driven into the subthreshold region, the frequency dependent characteristic is observed. This change of frequency dependence can be easily seen in Fig. 9. At Vg=1.0V, the power density is still very much constant with frequency. As Vg is less than Vt, the frequency dependence starts to appear and is especially obvious in the subthreshold region.

Unlike channel noise, induced gate noise is roughly proportional to the square of frequency. Fig. 10 shows how the power density changes with gate bias, Vg. The trend is actually very similar to that of the channel noise, except that it does not drop as fast as the channel noise with decreasing Vg.

The measurement results indicate that induced gate noise deviates the most from the models we've mentioned. It shows that more effort should be focused on how the diffusion current dominated subtreshold region affects the output noise. Simply using a drift model will not be enough. Also, better understanding of the gate coupling will be necessary for predicting the induced gate noise more accurately.

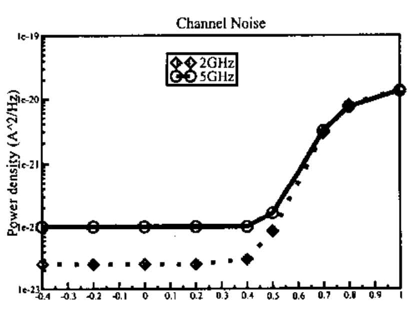

Fig. 8 Extracted power density of channel noise at 2GHz and 5GHz

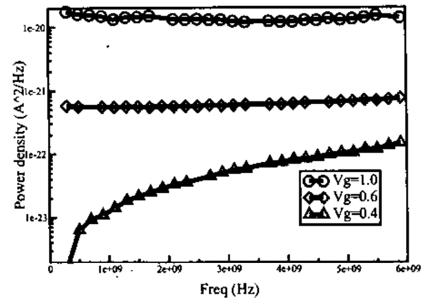

Fig. 9 Extracted power density of channel noise versus frequency

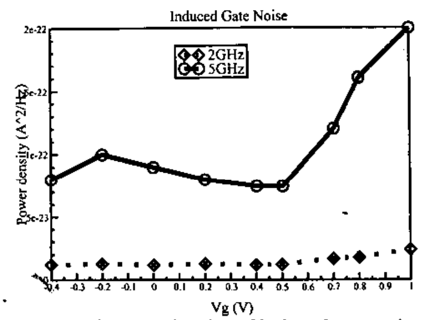

Fig. 10 Extracted power density of induced gate noise at 2GHz and 5GHz

SUMMARY

In this paper, we have shown the noise characteristics of 0.13um and 0.18um MOSFETs at various drain and gate bias. We have focused on the noise behavior of MOSFETs in the "off" state, a region that is becoming increasingly important and may have been overlooked in the past. Importantly, we show that the noise characteristic very much saturates in the subthreshold region, as opposed to the result most of the existing models predict.

ACKNOWLEDGEMENT

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